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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/002,031	11/30/2001	Yee-Chia Yeo	TS01-1132	5020

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EXAMINER
LATTIN, CHRISTOPHER W

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 05/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/002,031	Applicant(s) YEO ET AL.	
	Examiner Christopher W Lattin	Art Unit 2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-27 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 16-27 is/are allowed.

6)☒ Claim(s) 1-15 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In line 1 of claims 5-7 the limitation "silicon layer, underlying said SiGe layer" is recited. There is insufficient antecedent basis for this limitation in the claims. Claim 7 is further unclear due to the phrase "at a pressure between less than 200 mtorr.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3-5, 8, 11, 14, and 15 rejected under 35 U.S.C. 102(b) as being anticipated by Fischer et al. (U.S. Patent 6,111,267).

Fischer et al. teach a method of fabricating complementary metal oxide semiconductor (CMOS) devices on a semiconductor substrate, featuring a silicon - germanium (SiGe) layer 6 used as a component of a CMOS device channel region, with the integration of a selective epitaxially deposited, strained SiGe channel layer in a

CMOS process performed after formation of isolation regions, comprising the steps of providing a first region of said semiconductor substrate to be used as an NMOS region, and providing a second region of said semiconductor substrate to be used as a PMOS region; forming isolation regions 4 in top portions of said semiconductor substrate, forming a P well region 3 in said NMOS region, and forming an N well region 2 in said PMOS region; selectively depositing a composite undoped silicon layer on the top surface of portions of said semiconductor substrate not occupied by said isolation regions, with said composite silicon layer comprised of said SiGe layer grown to a thickness between about 20 to 150 Angstroms on an underlying silicon layer of 0 to 100 Angstroms, and an overlying silicon layer of 5 to 100 Angstroms, and forming a silicon dioxide gate insulator layer at a thickness between about 5 to 80 Angstroms on said overlying silicon layer.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fischer et al. (U.S. Patent 6,111,267) in view of Wolf, S. (Silicon Processing for the VLSI Era Volume 3: The Submicron MOSFET, Sunset Beach, CA, 1995, p.p. 367-373).

Fisher et al. are applied to claim 1 above and teach all of the limitations of claim 2, but fail to teach that isolation regions are insulator filled, shallow trench isolation regions. Wolf teaches that STI is a preferred method of isolation to LOCOS since bird's beak is entirely eliminated, channel-stop redistribution is reduced and smaller isolation spacing is possible.

Claims 6, 7, 9, 10, 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fischer et al. (U.S. Patent 6,111,267) in view of Kubo (U.S. Patent 6,190,975).

Fisher et al. are applied to claim 1 above and teach all of the limitations of claims 6,7,9,10, 12 and 13, but fail to specify using ultra-high vacuum chemical vapor deposition (UHV - CVD) procedures at a pressure between less than 200 mtorr, using silane or disilane as a source. Kubo et al. teach selectively growing silicon layers via ultra-high vacuum chemical vapor deposition (UHV - CVD) procedures at a temperature between about 400 to 800 °C, and at a pressure less than 200 mtorr using silane or disilane and germane reactants. It would have been obvious to one skilled in the art at the time of the invention selectively grow the silicon layers of Fischer et al. via ultra-high vacuum chemical vapor deposition (UHV - CVD) procedures at a temperature between about 400 to 800' C, and at a pressure less than 200 mtorr using silane or disilane and germane reactants as taught by Kubo et al. in order to grow a high quality silicon composite layer for use in a CMOS transistor.

Allowable Subject Matter

Claims 16-27 are allowed. The prior art of record fails to adequately anticipate or obviate either singularly or in combination with another reference a method of forming CNIOS devices featuring a channel region formed in a selectively grown, composite silicon layer, wherein said composite silicon layer is comprised of at least a strained SiGe layer and an overlying silicon layer, comprising the steps of providing a first region of said semiconductor substrate to be used as an NMOS region, and providing a second region of said semiconductor substrate to be used as a PMOS region, forming shallow trench isolation (STI) regions in top portions of said semiconductor substrate, with a top portion of each STI region featuring tapered sides, forming a P well region in a top portion of said NMOS region, and forming an N well region in a top portion of said PMOS region; *selectively depositing a composite silicon layer on the top surface of said P well region and on the top surface of said N well region, with said composite silicon layer featuring tapered sides, resulting in V-groove openings located between said tapered sides of said STI regions and tapered sides of said composite silicon layer*, and with said composite silicon layer comprised of a silicon layer, a strained SiGe layer, and an overlying silicon layer, *depositing an insulator layer; removing portion of insulator layer from the top surface of said composite insulator layer resulting in insulator filled V-grooves located between said STI regions and said composite silicon layer*, and thermally oxidizing a top portion of said overlying silicon layer to form a silicon dioxide gate insulator layer on a bottom portion of said overlying silicon layer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher Lattin whose telephone number is (703) 305-3017. The examiner can normally be reached Monday through Friday from 8:00 A.M. to 5:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling, can be reached at (703) 308-3325. The fax numbers for this Group are (703) 872-9318 for responses to non-final actions and (703) 872-9319 responses to final actions.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

CWL
May 20, 2003

John F. Niebling
Supervisory Patent Examiner
Technology Center 2800